REMARKS

Claims 1, 4-6, 8-14 and 16-20 have been amended. Claims 2, 9 and 15 have been cancelled. Claims 21 and 22 have been added. Claims 1-8, 10-14 and 16-22 are the pending claims in this application.

OBJECTIONS

The signed declaration filed with the pending application was objected to for the reasons noted in item 1 and 2 of the Office Action. A supplemental declaration, signed by the inventor, is filed herewith to obviate those objections.

The drawings stand objected to for the reasons noted at in items 4-6 of the Office Action. Corrected drawings are submitted herewith to obviate those objections. Specifically, FIG. 1 has been corrected to delineate the components that are included in computer 100, and a legend as "Prior Art". The corrections to FIG. 1 are supported by the description in the specification on page 1, lines 10-18. A legend as "Prior Art" has been added to FIG. 2. The correction to FIG. 2 is supported by the description in the specification on page 2, lines 3-15. FIG. 3 has been corrected to identify "pin 155". The correction to FIG. 3 is supported by the description in the specification on page 2, lines 3-15 and in the paragraph beginning at page 3, line 19. None of the corrections to the figures adds new matter.

Formal drawings are also being prepared and will be submitted as soon as possible.

The specification was objected to for reasons noted at item 7 of the Office Action. The specification has been amended to

address this objection and to attend to minor matters. No new matter has been added.

Claims 8 and 20 were objected to as containing grammatical errors. This contention has been obviated by the amendments made to claims 8 and 20.

SECTION 112 REJECTIONS

Claims 1, 2, 4-6, 9, 12-13 and 15-19 stand rejected under 35 U.S.C. §112, as being indefinite. The affected pending claims have been amended to obviate this rejection, in accordance with MPEP § 2173.05(b).

SECTION 102 AND 103 REJECTIONS

Claims 1, 3, 7, 8, 10, 14 and 16 are rejected under 35 U.S.C. §102(e) as being anticipated by Boaz et al.[USPN 6,061,263]. Claim 20 stands rejected under 35 U.S.C. §102(e) as being anticipated by Leddige et al.[USPN 6,115,205]. Claims 2, 9, and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] in view of Kumakura et al.[USPN 6,114,751]. Claims 4, 11, 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] as applied to claim 2 above, and further in view of Perino et al.[USPN 6,160,716]. Claims 5, 12 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] as applied to claim 4 above, and further in view of Perino et al.[USNP 6,160,716]. Claims 6, 13 and 19 are rejected under U.S.C. §103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] as applied to claim 5 above, and further in view of Holman et al.[USPN 6,005,776].

The present invention describes routing signal lines between a memory control unit and a memory unit that does not

require a ground trace line between the signal lines. See, for example, Figure 3 and the description at pages 3-5. The inventor found that a gap formed between neck down portions of each signal line provides an isolation between the signal lines yet reduces the area required to route the signal lines on a circuit board. Placing the gap, and not a ground trace, between the neck down portions may reduce congestion at the memory unit. This allows the signal lines into and out of the memory unit to be routed on a single layer of the circuit board on which the memory control unit (MCU) and the memory unit reside. Routing the signal lines in this manner may reduce the number of layers required to route signals between the MCU and the memory unit by a factor of two. As a result, the circuit board on which the MCU and memory unit reside can be less expensive to produce than conventional memory boards.

Boaz discloses an in-line memory module that uses "wrong-way" routing in order to match impedances of signal lines. Leddige discloses a connector having an array of vias using voltage traces that may vary in width. However, neither Boaz nor Leddige teaches or suggests "a circuit board having multiple layers and comprising: a first signal line, formed on a first layer of the circuit board … and a second signal line also formed on the first layer of the circuit board and connected to the first connection on the memory unit, a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the second signal line at an acute angle relative to a second portion of the first signal line, wherein said layer defines a non-grounded gap between said first and second lines", as recited by Applicant's exemplary claim 1.

None of the other art cited teaches or suggests "a circuit board having multiple layers and comprising: a first signal line, formed on a first layer of the circuit board … and a second signal line also formed on the first layer of the circuit board and connected to the first connection on the memory unit, a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the second signal line at an acute angle relative to a second portion of the first signal line, wherein said layer defines a non-grounded gap between said first and second lines", as recited by Applicant's exemplary claim 1.

Claims 8 and 20 are the other independent claims, having similar limitations to independent claim 1. In view of the foregoing distinctions, Applicant respectfully submits that independent claims 1, 8 and 20 are patentably distinguishable over the cited art. Applicant respectfully submits that claims 1, 8 and 20 are in condition for allowance, and Applicant respectfully requests allowance of claims 1, 8 and 20.

Claims 2-7, 10-14, 16-19 and 21-22 depend either directly or indirectly from one of the independent claims. Each dependent claim further defines the independent claim from which it depends. In view of the foregoing remarks regarding claims 1, 8 and 20, Applicant respectfully submit that claims 2-7, 10-14, 16-19 and 21-22 are likewise in condition for allowance. Applicant respectfully requests allowance of claims 2-7, 10-14, 16-19 and 21-22.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed. Enclosed is a $36.00 check for excess claim fees. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 8/7/02

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Version with markings to show changes made

In the specification:

Paragraph beginning at page 1, line 10 has been amended as follows:

-- FIG. 1 shows a typical computer system 100. The computer 100 includes a central processing unit (CPU) 105, or processor, and a memory repeater hub 110 ("memory unit" 110). A memory control unit (MCU) 120 controls the flow of data into and out of the memory unit 110. The memory unit 110 always includes volatile memory, such as dynamic random access memory (DRAM). The computer also includes other system components, including a non-volatile storage device, such as a hard disk 125, and a modem 130 to connect the computer 100 to a network 135. A bus 115 connects the components 105, 120, 125 and 130 of computer 100, allowing data and/or commands to be transferred between the components.--

Paragraph beginning at page 3, line 19 has been amended as follows:

-- FIG. 3 shows a signal routing configuration that reduces the area required for each signal line 200 running between the MCU 120 and the memory unit. In this configuration, the signal line 200 has a width of approximately 18 mils with a 5 mil neck down portion 205 contacting the corresponding pin 155[135] on the memory unit. The signal line 210 exiting the pin 155[135] also has a width of approximately 18 mils with a 5 mil neck down portion 215 contacting the pin 155[135]. The two neck down portions 205, 215 run substantially parallel to each other for a distance, and then at[act] an acute angle for another distance, the portions are separated by a gap 220. This gap 220 also has

a width of approximately 5 mils. The neck down portions 205, 215 are not separated by a ground trace. --

Paragraph beginning at page 5, line 1 has been amended as follows:

-- FIG. 4 shows the neck down portions 205, [215] of the signal line 200, and neck down portion 215 of signal line 210, on a multi-layer circuit board 225. The neck down portions 205, 215 into and out of the memory unit are formed on a single layer of the circuit board 225 and are separated by a gap 220 in which no traces are formed. No ground trace lies between the neck down portions [signal lines] 205, 215. In some embodiments, ground traces 230, 235 lie on either side of the [signal lines] neck down portions 205, 215 on the same layer of the circuit board 225. A ground plane 240 may lie[s] above or below the signal lines 200, 210 [205, 215] on another layer of the circuit board. --

In the claims:

claim 2, 9 and 15 has been cancelled.

claim 1, 4-6, 8-14 and 16-20 has been amended as follows:

1. (Amended) A computer system comprising:

a processor;

a memory unit configured to store data used by the processor;

a memory control unit configured to manage data flowing into and out of the memory unit;

a circuit board having multiple layers and comprising:

a first signal line, formed on a first layer of the circuit board and connected between a first connection on the memory unit and the memory control unit; and

a second signal line also formed on the first layer of the circuit board and connected to the first connection[pin] on the memory unit, a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the second signal line at an acute angle relative to a second portion of the first signal line,

wherein said layer defines a non-grounded gap between said first and second lines.

4. (Amended) The system of claim 1[2], wherein the first signal line and the portion of the second signal line that is routed substantially[roughly] parallel to the first signal line have substantially equal widths.

5. (Amended) The system of claim 4, wherein the first signal line and the portion of the second signal line that is routed substantially[roughly] parallel to the first signal line are separated by a distance approximately equal to said widths.

6. (Amended) The system of claim 5, wherein the widths of the lines and the distance separating the lines are each about [approximately] 5 mils.

8. (Amended) A method for use in routing signals between a memory unit and a memory control unit, the method comprising:

delivering a first signal over a first signal line formed on a selected layer of a circuit board and connected between the memory control unit and on the memory unit;

delivering a second signal over a second signal line formed on the selected layer of the circuit board and connected to the first connection[pin] of the memory unit, a first portion of the second signal line formed substantially parallel to a first portion of the first signal line, a second portion of the second signal line formed at an acute angle relative to a second portion of the first signal line; and

separating said first and second signal lines without a ground connection therebetween.

9. (Cancelled) The method of claim 8, wherein said delivering the second signal includes delivering the second signal over a portion of the second signal line that is routed roughly parallel to a portion of the first signal line.

10. (Amended) The method of claim 8, further comprising delivering another signal to said memory control unit on another layer of the circuit board over portions of the first and second signal lines that are not separated by any conductive traces.

11. (Amended) The method of claim 8, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that have substantially equal widths.

12. (Amended) The method of claim 11, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that

are separated by a distance substantially[approximately] equal to their widths.

13. (Amended) The method of claim 12, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that are about [approximately] 5 mils wide and that are separated by a distance of about[approximately] 5 mils.

14. (Amended) A method for use in manufacturing a computer system, the method comprising:

forming a multiple-layer circuit board with first and second signal lines on a selected layer of the board;

connecting a memory unit to the board such that a first connection on the memory unit connects to the first and second signal lines; [and]

affixing a memory control unit to the board such that the memory control unit connects to at least the first signal line[.];

forming a first portion of the second signal line to be substantially parallel to a first portion of the first signal line; and

forming a second portion of the second signal line to be at an acute angle relative to a second portion of the first signal line.

16. (Amended) The method of claim 14, further comprising forming the first and second signal[conductive] lines such that no conductive trace lies between the first signal line and the first portion of the second signal line that is routed roughly parallel to the first signal line.

17. (Amended) The method of claim 16, further comprising forming the first signal line and the first portion of the second signal line that is routed roughly parallel to the first signal line to have substantially equal widths.

18. (Amended) The method of claim 17, further comprising forming the first signal line and the first portion of the second signal line that is routed substantially[roughly] parallel to the first signal line to be separated by a distance approximately equal to their widths.

19. (Amended) The method of claim 18, further comprising forming the signal lines such that the widths of the lines and the distance separating the lines are all about equal to [approximately] 5 mils.

20. (Amended) A circuit board for use in a computer system comprising:

a memory unit;

a memory control unit; and

a data bus connecting the memory control unit to the memory unit and comprising:

a first signal line formed on a selected layer of the circuit board and connected to the memory control unit and to a first connection on the memory unit; and

a second signal line formed on the selected layer of the circuit board and also connected to the first connection on the memory control unit[.],a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the

second signal line at an acute angle relative to a second portion of the first signal line,

wherein said selected layer defines a non-grounded gap between said first and second lines.